AMENDMENTS TO THE CLAIMS

1. (Original) A data memory cache unit which is used between an arithmetic unit and a main memory unit accessed by the arithmetic unit, comprising:

a data holding section which includes a plurality of data areas for holding data, the data held in each of the plurality of data areas being read from and written in the main memory unit at one time, each of the plurality of data areas being divided into a plurality of small areas, and the data held in each of the plurality of small areas being read from and written in the arithmetic unit at one time; and

a control section in which, if there is a consecutive-writing demand from the arithmetic unit for writing of data into consecutive addresses of the main memory unit and if a cache miss takes place in an object data area which is the data area that corresponds to an address outputted by the arithmetic unit, then the object data area is opened, and thereafter, if an object small area which is the small area that corresponds to the address outputted by the arithmetic unit in the object data area is adjacent to a data area boundary which is the boundary of the object data area located in the direction where the consecutive writing is earlier executed with respect to the order of addresses, then refill of data is not executed into the object data area from the main memory unit, and the data outputted by the arithmetic unit is written into the object small area, and if the object small area is not adjacent to the data area boundary, then refill of data is executed into the object data area from the main memory unit, and the data outputted by the arithmetic unit is written into the object small area.

2. (Original) The data memory cache unit according to claim 1, wherein the control section includes:

a push-access detection portion which detects the consecutive-writing demand from the arithmetic unit;

a cache-miss decision portion which decides whether or not there is a cache miss with respect to the object data area if the push-access detection portion detects the consecutive-writing demand;

a boundary decision portion which decides whether or not the object small area is adjacent to the data area boundary if the push-access detection portion detects the consecutive-writing demand;

a data-area opening portion which opens the object data area if the cache-miss decision portion decides that a cache miss has taken place;

a refill portion which, in a case that the data-area opening portion opens the object data area, when the boundary decision portion makes a negative decision, refills data into the object data area opened by the data-area opening portion from the main memory unit, and when the boundary decision portion makes a positive decision, does not refill data into the object data area opened by the data-area opening portion from the main memory unit; and

a data writing portion which writes the data outputted by the arithmetic unit into the object small area if the push-access detection portion detects the consecutive-writing demand.

3. (Original) The data memory cache unit according to claim 2, wherein:

the data holding section further includes a plurality of valid-flag holding portions which hold a plurality of valid-flags that respectively show whether the plurality of data areas are opened or unopened; and

further in a case that the valid-flag which corresponds to the object data area is set to show the opening, when the boundary decision portion makes a negative decision, the refill portion refills data into the object data area from the main memory unit, and when the boundary decision portion makes a positive decision, the refill portion does not refill data into the object data area portion from the main memory unit.

4. (Original) The data memory cache unit according to claim 2, wherein:

the data holding section further includes a plurality of stack-flag holding portions which hold a plurality of stack-flags that respectively show whether the plurality of data areas have been used in either consecutive writing or consecutive read-out; and

the control section further includes a stack-flag setting portion which, when the boundary decision portion makes a positive decision, sets the stack-flag which

corresponds to the object data area on the positive side after the data writing portion finishes writing the data, and when the boundary decision portion makes a negative decision, does not change the stack-flag which corresponds to the object data area after the data writing portion finishes writing the data.

5. (Original) The data memory cache unit according to claim 2, wherein:

the plurality of data areas correspond to an intermediately significant digital part of the addresses of the main memory unit, each of the plurality of small areas corresponds to a less significant digital part of the addresses of the main memory unit, and one or more data areas correspond to the identical value of the intermediately significant digital part of the addresses of the main memory unit;

the data holding section further includes a plurality of tag holding portions which hold a plurality of tags that respectively show a more significant digital part of the addresses of the data held in the plurality of data areas;

the control section further includes an address extract portion which extracts the more significant digital part, the intermediately significant digital part and the less significant digital part from the address outputted by the arithmetic unit;

the cache-miss decision portion compares the value shown in the tag that corresponds to each of the one or more data areas which correspond to the intermediately significant digital part extracted by the address extract portion with the more significant digital part extracted by the address extract portion, and thereby, decides that a cache miss has taken place if there is no coincidence between them;

the boundary decision portion decides whether or not the small area that corresponds to the less significant digital part extracted by the address extract portion of the plurality of small areas is adjacent to the boundary located in the direction where the consecutive writing is earlier executed of the data area to which the small area belongs with respect to the order of addresses, and thereby, decides whether or not the object small area is adjacent to the data area boundary;

the data-area opening portion opens one of the one or more data areas that correspond to the intermediately significant digital part extracted by the address extract portion, if the push-access detection portion detects the consecutive-writing demand, and

if the cache-miss decision portion decides that a cache miss has taken place, and thereby, opens the object data area;

the control section further includes a tag updating portion which updates the tag that corresponds to the data area opened by the data-area opening portion, so that the tag comes to hold the more significant digital part extracted by the address extract portion; and

the data writing portion writes the data outputted by the arithmetic unit into the small area as the object small area, which corresponds to the less significant digital part extracted by the address extract portion in the data area that corresponds to the intermediately significant digital part extracted by the address extract portion and corresponds to the tag which holds the more significant digital part extracted by the address extract portion.

6. (Canceled)

7. (Currently Amended) A data memory cache unit which is used between an arithmetic unit and a main memory unit accessed by the arithmetic unit, comprising:

a data holding section which includes a plurality of data areas that correspond to addresses of the main memory unit and hold the data on the corresponding addresses; and

a control section in which, if consecutive read-out is executed which is read-out of data from consecutive addresses of the main memory unit to the arithmetic unit, then opens the data area in which the consecutive read-out is completed of the data holding section, without writing back to the main memory unit the data held in the data area in which the consecutive read-out is completed;~~The data memory cache unit according to claim 6, wherein:~~

wherein:

the data held in each of the plurality of data areas is read from and written in the main memory unit at one time, each of the plurality of data areas is divided into a plurality of small areas, and the data held in each of the plurality of small areas is read from and written in the arithmetic unit at one time; and

the control section, if there is a consecutive read-out demand from the arithmetic unit for the read-out of data from consecutive addresses of the main memory unit, then reads out data to the arithmetic unit from an object small area which is the small area that corresponds to the address outputted by the arithmetic unit in an object data area which is the data area that corresponds to the address outputted by the arithmetic unit, and ~~besides,~~ if the object small area is adjacent to a data area boundary which is the boundary of the object data area located in the direction where the consecutive read-out is later executed with respect to the order of addresses, then opens the object data area without writing the data back to the main memory unit from the object data area, and if the object small area is not adjacent to the data area boundary, then does not open the object data area.

8. (Original) The data memory cache unit according to claim 7, wherein:

the data holding section further includes a plurality of valid-flag holding portions which hold a plurality of valid-flags that respectively show whether the plurality of data areas are opened or unopened; and

the control section sets the valid-flag which corresponds to the object data area to show the opening, and thereby, opens the object data area.

9. (Original) The data memory cache unit according to claim 8, wherein the control section includes:

a pop-access detection portion which detects the consecutive read-out demand from the arithmetic unit;

a boundary decision portion which decides whether or not the object small area is adjacent to the data area boundary if the pop-access detection portion detects the consecutive read-out demand;

a data read-out portion which reads out the data of the object small area to the arithmetic unit if the pop-access detection portion detects the consecutive read-out demand; and

a valid-flag setting portion which, when the boundary decision portion makes a positive decision, after the data read-out portion reads out the data, sets the valid-flag which corresponds to the object data area to show the opening without writing the data

back to the main memory unit from the object data area, and if the object small area is not adjacent to the data area boundary, does not change the valid-flag which corresponds to the object data area.

10. (Original) The data memory cache unit according to claim 9, wherein:

the data holding section further includes a plurality of stack-flag holding portions which hold a plurality of stack-flags that respectively show whether the plurality of data areas have been used in either consecutive writing or consecutive read-out; and

the control section further includes a stack-flag setting portion which, when the boundary decision portion makes a positive decision, sets the stack-flag which corresponds to the object data area on the positive side after the data read-out portion finishes reading out the data, and when the boundary decision portion makes a negative decision, does not change the stack-flag which corresponds to the object data area after the data read-out portion finishes reading out the data.

11. (Original) The data memory cache unit according to claim 9, wherein:

the plurality of data areas correspond to an intermediately significant digital part of the addresses of the main memory unit, each of the plurality of small areas corresponds to a less significant digital part of the addresses of the main memory unit, and one or more data areas correspond to the identical value of the intermediately significant digital part of the addresses of the main memory unit;

the data holding section further includes a plurality of tag holding portions which hold a plurality of tags that respectively show a more significant digital part of the addresses of the data held in the plurality of data areas;

the control section further includes an address extract portion which extracts the more significant digital part, the intermediately significant digital part and the less significant digital part from the address outputted by the arithmetic unit;

the boundary decision portion decides whether or not the small area that corresponds to the less significant digital part extracted by the address extract portion of the plurality of small areas is adjacent to the boundary located in the direction where the consecutive read-out is later executed of the data area to which the small area belongs with respect to

the order of addresses, and thereby, decides whether or not the object small area is adjacent to the data area boundary; and

the data read-out portion reads out the data of the small area as the object small area to the arithmetic unit, which corresponds to the less significant digital part extracted by the address extract portion in the data area that corresponds to the intermediately significant digital part extracted by the address extract portion and corresponds to the tag which holds the more significant digital part extracted by the address extract portion.

12. (Currently Amended) A data memory cache unit which is used between an arithmetic unit and a main memory unit accessed by the arithmetic unit, comprising:

a data holding section which includes a plurality of data areas for holding data, the data held in each of the plurality of data areas being read from and written in the main memory unit at one time, each of the plurality of data areas being divided into a plurality of small areas, and the data held in each of the plurality of small areas being read from and written in the arithmetic unit at one time; and

a control section in which, if there is a consecutive read-out demand from the arithmetic unit for the read-out of data from consecutive addresses of the main memory unit, then data is read out to the arithmetic unit from an object small area which is the small area that corresponds to the address outputted by the arithmetic unit in an object data area which is the data area that corresponds to the address outputted by the arithmetic unit, and ~~besides,~~ if the object small area is adjacent to a data area boundary which is the boundary of the object data area located in the direction where the consecutive read-out is later executed with respect to the order of addresses, a setting is executed for inhibiting data from being written back to the main memory unit from the object data area when the object data area is opened, and if the object small area is not adjacent to the data area boundary, then the setting is not executed.

13. (Original) The data memory cache unit according to claim 12, wherein:

the data holding section further includes a plurality of dirty-flag holding portions which hold a plurality of dirty-flags that respectively show whether or not the data held in

the plurality of data areas coincides with the data held in the corresponding address by the main memory unit; and

the control section, to execute the setting, sets the dirty-flag which corresponds to the object data area to show the coincidence.

14. (Original) The data memory cache unit according to claim 13, wherein the control section includes:

a pop-access detection portion which detects the consecutive read-out demand from the arithmetic unit;

a boundary decision portion which decides whether or not the object small area is adjacent to the data area boundary if the pop-access detection portion detects the consecutive read-out demand;

a data read-out portion which reads out the data of the object small area to the arithmetic unit if the pop-access detection portion detects the consecutive read-out demand; and

a dirty-flag setting portion which, when the boundary decision portion makes a positive decision, after the data read-out portion reads out the data, sets the dirty-flag which corresponds to the object data area to show the coincidence, and when the boundary decision portion makes a negative decision, does not change the dirty-flag which corresponds to the object data area.

15. (Original) The data memory cache unit according to claim 14, wherein:

the data holding section further includes a plurality of stack-flag holding portions which hold a plurality of stack-flags that respectively show whether the plurality of data areas have been used in either consecutive writing or consecutive read-out; and

the control section further includes a stack-flag setting portion which, when the boundary decision portion makes a positive decision, sets the stack-flag which corresponds to the object data area on the positive side after the data read-out portion finishes reading out the data, and when the boundary decision portion makes a negative decision, does not change the stack-flag which corresponds to the object data area after the data read-out portion finishes reading out the data.

16. (Original) The data memory cache unit according to claim 14, wherein:

the plurality of data areas correspond to an intermediately significant digital part of the addresses of the main memory unit, each of the plurality of small areas corresponds to a less significant digital part of the addresses of the main memory unit, and one or more data areas correspond to the identical value of the intermediately significant digital part of the addresses of the main memory unit;

the data holding section further includes a plurality of tag holding portions which hold a plurality of tags that respectively show a more significant digital part of the addresses of the data held in the plurality of data areas;

the control section further includes an address extract portion which extracts the more significant digital part, the intermediately significant digital part and the less significant digital part from the address outputted by the arithmetic unit;

the boundary decision portion decides whether or not the small area that corresponds to the less significant digital part extracted by the address extract portion of the plurality of small areas is adjacent to the boundary located in the direction where the consecutive read-out is later executed of the data area to which the small area belongs with respect to the order of addresses, and thereby, decides whether or not the object small area is adjacent to the data area boundary; and

the data read-out portion reads out the data of the small area as the object small area to the arithmetic unit, which corresponds to the less significant digital part extracted by the address extract portion in the data area that corresponds to the intermediately significant digital part extracted by the address extract portion and corresponds to the tag which holds the more significant digital part extracted by the address extract portion.

17. (Original) A data memory cache unit which is used between an arithmetic unit and a main memory unit accessed by the arithmetic unit, comprising:

a data holding section which includes a plurality of data areas that correspond to addresses of the main memory unit and hold the data on the corresponding addresses; and

a control section which, during the period when consecutive writing is executed which is writing of data into consecutive addresses of the main memory unit from the

arithmetic unit and during the period when a data bus for transferring data between the data holding section and the main memory unit is not in operation, writes the data back to the main memory unit from the data area in the data holding section which is located in the direction where the consecutive writing is earlier executed than the consecutive writing that is presently executed with respect to the order of addresses.

18. (Original) The data memory cache unit according to claim 17, wherein the control section includes:

a push-access detection portion which detects the consecutive-writing demand from the arithmetic unit;

an offset calculation portion which, if the push-access detection portion detects the consecutive-writing demand, then calculates an offset address that is the address located a predetermined distance apart in the direction where the consecutive writing is earlier executed from the address outputted by the arithmetic unit;

a cache-miss decision portion which decides whether or not there is a cache miss with respect to the offset address;

a transfer-busy decision portion which decides whether or not the data bus is in operation; and

a write-back portion which, if the cache-miss decision portion decides that there is no cache miss and if the transfer-busy decision portion decides that the data bus is not in operation, writes the data back to the main memory unit from the data area which corresponds to the offset address.

19. (Original) The data memory cache unit according to claim 18, wherein:

the plurality of data areas correspond to an intermediately significant digital part of the addresses of the main memory unit, and one or more data areas correspond to the identical value of the intermediately significant digital part;

each of the plurality of data areas is divided into a plurality of small areas which corresponds to a less significant digital part of the address;

the data held in each of the plurality of data areas is read from and written in the main memory unit at one time, and the data held in each of the plurality of small areas is read from and written in the arithmetic unit at one time;

the data holding section further includes a plurality of tag holding portions which hold a plurality of tags that respectively show a more significant digital part of the addresses of the data held in the plurality of data areas;

the control section further includes an address extract portion which extracts the more significant digital part, the intermediately significant digital part and the less significant digital part from the address outputted by the arithmetic unit;

the offset calculation portion, if the push-access detection portion detects the consecutive-writing demand, then calculates as the offset address the address located a predetermined distance apart in the direction where the consecutive writing is earlier executed from the address represented with the intermediately significant digital part and the more significant digital part that are extracted by the address extract portion; and

the cache-miss decision portion compares the value shown in the tag that corresponds to each of the one or more data areas which correspond to the intermediately significant digital part of the offset address with the more significant digital part of the offset address, and thereby, decides that a cache miss has taken place if there is no coincidence between them.

20. (Original) The data memory cache unit according to claim 18, wherein:

the data holding section further includes a plurality of stack-flag holding portions which hold a plurality of stack-flags that respectively show whether or not the plurality of data areas have been used in either consecutive writing or consecutive read-out; and

if the cache-miss decision portion decides that there is no cache miss and if the transfer-busy decision portion decides that the data bus is not in operation, and in addition, only when the stack-flag which corresponds to the data area that corresponds to the offset address is set on the positive side, the write-back portion writes the data back to the main memory unit from the data area which corresponds to the offset address.

21. (Original) The data memory cache unit according to claim 18, wherein:

the data holding section further includes a plurality of valid-flag holding portions which hold a plurality of valid-flags that respectively show whether the plurality of data areas are opened or unopened; and

if the cache-miss decision portion decides that there is no cache miss and if the transfer-busy decision portion decides that the data bus is not in operation, and in addition, only when the valid-flag which corresponds to the data area that corresponds to the offset address is set on the unopened side, the write-back portion writes the data back to the main memory unit from the data area which corresponds to the offset address.

22. (Original) A data memory cache unit which is used between an arithmetic unit and a main memory unit accessed by the arithmetic unit, comprising:

a data holding section which includes a plurality of data areas that correspond to addresses of the main memory unit and hold the data on the corresponding addresses; and

a control section which, during the period when consecutive read-out is executed which is read-out of data from consecutive addresses of the main memory unit to the arithmetic unit and during the period when a data bus for transferring data between the data holding section and the main memory unit is not in operation, writes the data back to the main memory unit from the data area in the data holding section which is located in the direction where the consecutive writing is earlier executed than the consecutive writing that is presently executed with respect to the order of addresses.

23. (Original) The data memory cache unit according to claim 22, wherein the control section includes:

a pop-access detection portion which detects the consecutive read-out demand from the arithmetic unit;

an offset calculation portion which, if the pop-access detection portion detects the consecutive read-out demand, then calculates an offset address that is the address located a predetermined distance apart in the direction where the consecutive read-out is earlier executed from the address outputted by the arithmetic unit;

a cache-miss decision portion which decides whether or not there is a cache miss with respect to the offset address;

a transfer-busy decision portion which decides whether or not the data bus is in operation; and

a write-back portion which, if the cache-miss decision portion decides that there is no cache miss and if the transfer-busy decision portion decides that the data bus is not in operation, writes the data back to the main memory unit from the data area which corresponds to the offset address.

24. (Original) The data memory cache unit according to claim 23, wherein:

the plurality of data areas correspond to an intermediately significant digital part of the addresses of the main memory unit, and one or more data areas correspond to the identical value of the intermediately significant digital part;

each of the plurality of data areas is divided into a plurality of small areas which corresponds to a less significant digital part of the address;

the data held in each of the plurality of data areas is read from and written in the main memory unit at one time, and the data held in each of the plurality of small areas is read from and written in the arithmetic unit at one time;

the data holding section further includes a plurality of tag holding portions which hold a plurality of tags that respectively show a more significant digital part of the addresses of the data held in the plurality of data areas;

the control section further includes an address extract portion which extracts the more significant digital part, the intermediately significant digital part and the less significant digital part from the address outputted by the arithmetic unit;

the offset calculation portion, if the pop-access detection portion detects the consecutive read-out demand, then calculates as the offset address the address located a predetermined distance apart in the direction where the consecutive read-out is earlier executed from the address represented with the intermediately significant digital part and the more significant digital part that are extracted by the address extract portion; and

the cache-miss decision portion compares the value shown in the tag that corresponds to each of the one or more data areas which correspond to the intermediately significant digital part of the offset address with the more significant digital part of the

offset address, and thereby, decides that a cache miss has taken place if there is no coincidence between them.

25. (Original) The data memory cache unit according to claim 23, wherein:

the data holding section further includes a plurality of stack-flag holding portions which hold a plurality of stack-flags that respectively show whether or not the plurality of data areas have been used in either consecutive writing or consecutive read-out; and

if the cache-miss decision portion decides that there is no cache miss and if the transfer-busy decision portion decides that the data bus is not in operation, and in addition, only when the stack-flag which corresponds to the data area that corresponds to the offset address is set on the positive side, the write-back portion writes the data back to the main memory unit from the data area which corresponds to the offset address.

26. (Original) The data memory cache unit according to claim 23, wherein:

the data holding section further includes a plurality of valid-flag holding portions which hold a plurality of valid-flags that respectively show whether the plurality of data areas are opened or unopened; and

if the cache-miss decision portion decides that there is no cache miss and if the transfer-busy decision portion decides that the data bus is not in operation, and in addition, only when the valid-flag which corresponds to the data area that corresponds to the offset address is set on the unopened side, the write-back portion writes the data back to the main memory unit from the data area which corresponds to the offset address.

27. (Original) A data memory cache unit which is used between an arithmetic unit and a main memory unit accessed by the arithmetic unit, comprising:

a data holding section which includes a plurality of data areas that correspond to addresses of the main memory unit and hold the data on the corresponding addresses; and

a control section which, during the period when consecutive read-out is executed which is read-out of data from consecutive addresses of the main memory unit to the arithmetic unit and during the period when a data bus for transferring data between the data holding section and the main memory unit is not in operation, refills data from the

main memory unit into the data area in the data holding section which is located in the direction where the consecutive read-out is later executed than the consecutive read-out that is presently executed with respect to the order of addresses.

28. (Original) The data memory cache unit according to claim 27, wherein the control section includes:

a pop-access detection portion which detects the consecutive read-out demand from the arithmetic unit;

an offset calculation portion which, if the pop-access detection portion detects the consecutive read-out demand, then calculates an offset address that is the address located a predetermined distance apart in the direction where the consecutive read-out is later executed from the address outputted by the arithmetic unit;

a transfer-busy decision portion which decides whether or not the data bus is in operation; and

a refill portion which refills data from the main memory unit into the data area which corresponds to the offset address if the transfer-busy decision portion decides that the data bus is not in operation.

29. (Original) The data memory cache unit according to claim 28, wherein:

the data holding section further includes a plurality of stack-flag holding portions which hold a plurality of stack-flags that respectively show whether the plurality of data areas have been used in either consecutive writing or consecutive read-out; and

if the transfer-busy decision portion decides that the data bus is not in operation, and in addition, only when the stack-flag which corresponds to the data area that corresponds to the offset address is set on the positive side, the refill portion refills data into the data area which corresponds to the offset address from the main memory unit.

30. (Original) The data memory cache unit according to claim 28, wherein:

the data holding section further includes a plurality of valid-flag holding portions which hold a plurality of valid-flags that respectively show whether the plurality of data areas are opened or unopened; and

if the transfer-busy decision portion decides that the data bus is not in operation, and in addition, only when the valid-flag which corresponds to the data area that corresponds to the offset address is set to show the opening, the refill portion refills data into the data area which corresponds to the offset address from the main memory unit.

31. (Original) The data memory cache unit according to claim 28, wherein:

the plurality of data areas correspond to an intermediately significant digital part of the addresses of the main memory unit, and one or more data areas correspond to the identical value of the intermediately significant digital part;

each of the plurality of data areas is divided into a plurality of small areas which corresponds to the less significant digital part of the address;

the data held in each of the plurality of data areas is read from and written in the main memory unit at one time, and the data held in each of the plurality of small areas is read from and written in the arithmetic unit at one time;

the data holding section further includes a plurality of tag holding portions which hold a plurality of tags that respectively show the more significant digital part of the addresses of the data held in the plurality of data areas;

the control section further includes an address extract portion which extracts the more significant digital part, the intermediately significant digital part and the less significant digital part from the address outputted by the arithmetic unit;

the offset calculation portion, if the pop-access detection portion detects the consecutive read-out demand, then calculates as the offset address the address located a predetermined distance apart in the direction where the consecutive read-out is later executed from the address represented with the intermediately significant digital part and the more significant digital part that are extracted by the address extract portion.

32. (Original) The data memory cache unit according to claim 31, wherein the control section further includes:

a cache-miss decision portion which compares the value shown in the tag that corresponds to each of the one or more data areas which correspond to the intermediately significant digital part of the offset address with the more significant digital part of the

offset address, decides that a cache miss has taken place with the offset address if there is no coincidence between them;

a data-area opening portion which opens one of the one or more data areas which correspond to the intermediately significant digital part of the offset address if the cache-miss decision portion decides that a cache miss has taken place; and

a tag updating portion which updates the tag that corresponds to the data area opened by the data-area opening portion, so that the tag comes to hold the more significant digital part of the offset address.

33. (Original) A data memory cache system, comprising:

a data memory cache unit which is used between an arithmetic unit and a main memory unit accessed by the arithmetic unit, comprising:

a data holding section which includes a plurality of data areas for holding data, the data held in each of the plurality of data areas being read from and written in the main memory unit at one time, each of the plurality of data areas being divided into a plurality of small areas, and the data held in each of the plurality of small areas being read from and written in the arithmetic unit at one time; and

a control section in which, if there is a consecutive-writing demand from the arithmetic unit for writing of data into consecutive addresses of the main memory unit and if a cache miss takes place in an object data area which is the data area that corresponds to an address outputted by the arithmetic unit, then the object data area is opened, and thereafter, if an object small area which is the small area that corresponds to the address outputted by the arithmetic unit in the object data area is adjacent to a data area boundary which is the boundary of the object data area located in the direction where the consecutive writing is earlier executed with respect to the order of addresses, then refill of data is not executed into the object data area from the main memory unit, and the data outputted by the arithmetic unit is written into the object small area, and if the object small area is not adjacent to the data area boundary, then refill of data is executed into the object data area from the main memory unit, and the data outputted by the arithmetic unit is written into the object small area;

an arithmetic unit which is connected to the data memory cache unit; and

a main memory unit which is connected to the data memory cache unit and is accessed by the arithmetic unit.